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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/338,286
Filing Date: June 22, 1999
Appellant(s): SNOW ET AL.

David P. Olynick
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 26, 2005 appealing from the Office action mailed December 8, 2004.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,071,190	Weiss	6-2000
5,788,509	Byers	8-1988

Newton, Harry "Newton Telecom Dictionary" 1998, p. 751.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 10, 11, 15, 16, 20, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509. The rejections contained in the previous office actions are maintained and incorporated herein. Weiss discloses all of the instant application without specifically disclosing how the various processing subsystems are connected such as the use of a motherboard with expansion slots and a serial UART. Weiss teaches a plurality of processors connected by a serial or parallel link or a motherboard with separate tasks performed whereby critical gaming functions may be partitioned from other functions by executing critical gaming functions on a separate dedicated processor and partitioning the devices hardware so that the functions not deemed critical which are stored or executed from alterable media are not capable of directly modifying the random access memory used by the critical gaming function. Further Weiss discloses in column 4 that any component required to be uniquely controlled by the critical gaming functions are preferably not accessible by other functions stored or executed from alterable media. Thus the non-alterable media containing the critical gaming functions is easily verifiable as to content independent of any function of the gaming device itself. In column 2 of Weiss it is disclosed that a need exists for an independent secured processor design for validation which would provide all key functions such as the determination of game outcome, monetary input, output, and logging of relevant events. Furthermore, a need exists for an open architecture design, for example, a personal computer based design (with respect to claim 20) of the gaming device which would provide all shell functions of presenting the game environment and thus providing a substantial

entertainment component of the gaming device. Weiss teaches that it is obvious to use a plurality of processing platforms constructed to be in communication with each other to provide security and be expandable for other gaming functions. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Weiss to connect the various processing systems such as by using a personal computer based design. With respect to claim 10 please see figure 2, figure 6 and column 6, 11, and 12 which disclose a housing 100, a plurality of user inputs, a display 50, a gaming processing subsystem is a secure processing area 60 which includes a processor board 162 and a main board 164 which controls the display and sound generated connected by a bus to a back plane 166. Board 164 also encompasses the general computing subsystem and has a bus interface and an expansion board. The processor board 162, a main board 164 and the back plane 166 may be integrally or separately formed. The main board includes memory in the form of ROM and EEPROM which can be non-volatile memory as disclosed in column 11. The use of PCI, ISA, VME, or AGP in order to connect peripherals to a bus are well known standards in the computing arts and will be treated as analogous interface protocols. With respect to claim 11 column 12 and figure 7 disclose a second gaming processing subsystem board 252, furthermore, the first gaming processing subsystem board controls the one or more features as outlined above. With respect to claim 15, column 11 discloses serial interface for linking with a second processing area and figure 6 which discloses a back plane for connection to peripherals and a plurality of communication ports. With respect to claims 16, and 21-23 Weiss discloses in columns 11 and 12 that the main board 164 is connected to another board 162, in addition the main board has a random number generator associated with it, and the main board has a back plane 166 which is integrally or

separately formed. Column 12 lines 30-35 disclose that the processor board also allows peripherals in the form of, for example, hard drives, CD ROMS, network interfaces, sound cards, ***and other desirable peripherals for game enhancement and patron entertainment (emphasis added)***. In an analogous invention to Byers et al teaches that it is known to attach to a motherboard Industry Standard Architecture (ISA) expansion cards that connect the computer electronics to the peripheral device. With respect to claim 16 a PCI expansion card meets the definition of an ISA expansion card. Therefore, It would be obvious to one of ordinary skill in the art at the time of the invention to have a pc computer with a motherboard capable of accepting cards using the motivation provided by Weiss that a computer backplane could be integrally or separately formed on the main board (motherboard) and that other desired peripherals for game enhancement and patron entertainment could be added to the main board.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509 as applied to the claims above and further in view of Newton's Telecom Dictionary page 751 the definition of UART. Weiss and Byers discloses all of the instant application as disclosed above but lack in disclosing the specific use of a serial UART as disclosed in claims 22 and 23. Instead Weiss discloses that the processor board also allows peripherals in the form of, for example, hard drives, CD ROMS, network interfaces, sound cards, and other desirable peripherals for game enhancement and patron entertainment. In this case it would be obvious to one of ordinary skill in the art to use a UART for game enhancement since Weiss already uses serial and parallel communications and the a UART would be used in order to simplify those communications which are already part of a communication port.

(10) Response to Argument

The rejection of claims 10, 11, 15, 16, 20, 21, and 24 under 35 U.S.C. § 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509.

Appellant begins the argument by attempting to describe what Weiss teaches; however, the Examiner respectfully disagrees with Appellant's description. For instance, Appellant alleges Weiss teaches, "a hardware architecture for computing on a gaming machine. Weiss describes **two processing areas linked together**: 1)a traditional gaming computing area with a main board ("motherboard"), including associated sub-boards, that is connected to a backplane and 2) a multimedia PC with a motherboard."

First, the Examiner agrees with the language provided by Appellant bolded above. Weiss discloses two processing areas linked together, the first (secure) processing area (20) that includes a random number generator, an accounting an log means operatively coupled to a static or non-volatile random access memory and an EPROM having stored therein the critical gaming functions and a second (open architecture) processing area (60) that is linked to the first (secure) processing area (20) and communicating therewith via the secure protocol. Additionally, a display means is operatively coupled to a visual display for displaying random outcomes. The first and second processing areas are depicted in Figure 1. Additionally, the first (secure) processing area (20) is depicted in more detail in Figure 6, whereas, the second (open architecture) processing area (60) is depicted in more detail in Figure 7.

Second, Appellant alleges both the first and second processing areas include motherboards and are linked together. The Examiner notes Appellant has not supplied any

reference to any drawings, to any specific citation in Weiss or otherwise to prove this allegation. Nowhere does Weiss even mention the term "motherboard" (nor does Appellant's disclosure either). At best, the first (secure) processing area (20), more fully depicted in Figure 6, which shows a "Main Board" (164) could equate to a "Motherboard." However, the Examiner does not see how Appellant can assert the same with regards to the second (open architecture) processing area (60), depicted in more detail in Figure 7. The second (open architecture) processing area (60), comprises a processor board (252) with no mention of the processing board being a "motherboard" or a "main board." For these reasons alone, the Examiner maintains the combination of Weiss (US Patent 6,071,190) in view of (Byers et al US Patent 5,788,509) taken as a whole to one having ordinary skill in the art at the time of Appellant's invention renders the claims obvious.

Appellant alleges first (secure) processing area (20) and second (open architecture) processing area (60) are two computers with two motherboards that are capable of functioning independently. The Examiner respectfully disagrees. To the contrary, the first processing area and the second processing area have a master/slave configuration in at least one regard. For example, the second processing area is the master communication device and initiates all messages. The first processing area is the slave and transmits data only when polled from the master (Column 10, lines 35-38). For this reasons alone, the Examiner maintains the combination of Weiss (US Patent 6,071,190) in view of (Byers et al US Patent 5,788,509) taken as a whole to one having ordinary skill in the art at the time of Appellant's invention renders the claims obvious.

Appellant alleges the combination of Weiss (US Patent 6,071,190) in view of (Byers et al US Patent 5,788,509) teaches away from the present invention. The Examiner respectfully disagrees for at least two reasons. First, Weiss discloses that it is desirable to use a PC based platform but it may not be an advantage due to security issues. This is not a statement that this sort of arrangement of parts is not viable, just not recommended. Second, the security features of the Appellant's arrangement are not claimed. For this reason, the Examiner maintains the combination of Weiss (US Patent 6,071,190) in view of (Byers et al US Patent 5,788,509) taken as a whole to one having ordinary skill in the art at the time of Appellant's invention renders the claims obvious.

The rejection of claims 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509 as applied to the claims above and further in view of Newton's Telecom Dictionary page 751 the definition of UART.

Appellant's allege claims 22 and 23 are patentable for the reasons presented above in regards to the patentability of claim 10. Your Honors, please see the argument provided above with regards to the rejection of claims 10, 11, 15, 16, 20, 21, and 24 under 35 U.S.C. § 103(a) as being unpatentable over Weiss US Patent 6,071,190 in view of Byers et al US Patent 5,788,509.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Scott E. Jones

Art Unit 3714, Primary Examiner

SCOTT JONES
PRIMARY EXAMINER

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